minimalFab
— using half-inch wafers to reduce a fab investment to 1/1,000

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Issues in enlarging silicon wafer

(1) Huge investment
(2) Enormous waste
(3) Valley of death in R&D

Estimated by a chip size of 1cm²

1975~
1980~
1991~
2001~
2020?

4”
6”
8”
12”

80chips
180chips
300chips
700chips
1600chips

MAGA-trend
(3) The Valley of Death in R&D

In this Minimal way, we can shrink the fab size.

Minimal Way

Research = Manufacture

(1) Research sample size
(2) High quality control by local clean technology

High Risk High Investment
Low Investment cost

Industrial Implementation Directly to the research facility

Valley of Death

Cost of R&D for to Manufacturing

Market

Factory

Industrial Research Section

Pure Science and Engineering

Mega Manufacturing
To what degree do we shrink the fab size?

In device fabs,

<table>
<thead>
<tr>
<th>Number of WIP product types at a certain moment</th>
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<tbody>
<tr>
<td>→  ~ 1,000 types @ a moment</td>
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1 type at a certain moment is an ideal fab.

Therefore, we make a fab of 1/1,000.

We call this fab of 1/1,000 “Minimal Fab”.

→ We use a tiny wafer intentionally.
Trend to enlarge silicon wafer

- 4” (80 chips, 1975~)
- 6” (180 chips, 1980~)
- 8” (300 chips, 1991~)
- 12” (1600 chips, 2001~)
- 18” (1600 chips, 2020?)
- 0.5” (1 chip, 2010~)

Estimated by a chip size of 1cm²

MAGA-trend

 Minimal way

Fab System Research Consortium, AIST
Scaling down of fabrication factory

Traditional MAGA FAB

- Fab investment: 5B$
- Wafer size: 12"
- Length: 200m
- Width: 2m
- No clean room

Room-sized Minimal FAB

- Fab investment: 5M$
- Wafer size: 0.5"
- Length: 10m
- Width: 0.3m
- 1/1,000 scale
- No clean room

Fab System Research Consortium, AIST
7 Cost trends for production volumes

Chip Prices [$/cm²]

Life Production Volumes of Chips

Prices of Consumer Products [$]

1. No one wants to produce under 10,000 chips.
2. Businesses of Minimal fab
3. Price zone of Major products
4. Volume Target
5. Advanced Target
6. Global Market
7. Variable Cost

Fabrication Design rules:
- 40nm
- 60nm
- 90nm
- 130nm
- 180nm
- 250nm

Yearly capacity of Minimal fab

100B$/year
100B$/year

Typical mass production effect
Standardized Wafer Transfer system

PLAD: Particle Lock Air-tight Docking system

Minimal Hermetic Seal Transfer System

Production / Development

Ultra rapid RD, and P

Research

Minimal Analyzer
Minimal Inspection
Minimal Specific process
Minimal Specific Process
Minimal High-tech. Fabrication
Minimal High-tech. Process
Minimal High-tech. Analyzer

Minimal Wet Cleaner
Minimal CVD
Minimal Coat./Dev.
Minimal Lithography
Minimal Plasma
Minimal I/I
Minimal High-tech. Analyzer

Minimal PLAD
minimal PLAD
minimal PLAD
minimal PLAD
minimal PLAD
minimal PLAD
minimal PLAD
minimal PLAD

30cm

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PLAD: Particle Lock Air-tight Docking
Minimal Tool, Wafer, Shuttle

Half inch wafer: \( \phi 12.5\text{mm} \)

Minimal Shuttle

4cm
Localized clean system for minimal fab

A front chamber where particles are absolutely protected during opening process of a shuttle

PLAD: Particle Lock Air-tight Docking

- No cleanwear
- No cleanroom

Localized clean system (EPS: Encapsulated Production System)
Measured Clean level of the system

Particle number data of minimal system and environment

- Exhibition Area $N=8.79$
  - ISO Class 9
- Office Room Area $N=8.38$
  - ISO Class 9
- Process Chamber $N=3.72$
  - ISO Class 4
- Wafer loadlock system (PLAD) $N=3.58$
  - ISO Class 4

Particle counter: KC-22B (RION)
Mask-less DLP Exposure

Wet Cleaning → Deposition → Coating → Exposure → Development → Etching → Resist Removal

Resist: TOK, OFPR-5000 4000rpm, 25sec ~1.00 micron, Develop: NMD-3 35sec

Imperfect process Area 0.50mm
Non coating area 0.28mm

Resist pattern after exposure

No particle without clean room.
In order to construct a minimal fab, we have to develop:

1. Materials, Parts, Modules
2. Process equipment
3. Process technologies
4. Devices
5. Factory system
Eco-system in minimal fab

Device makers, Minimal Fab Users
- Hitachi
- Toshiba NEC
- Yokogawa EL
- Omron
- TDK
- JTEKT
- Hamamatsu Photonics
- Renesas Semi. Manufacturing

Rikenkeiki
- Epoch transport
- Yamaha Solution Service
- Panasonic Factory Solutions
- TAMURA
- YAZAKI

KOYU
- Sanyo
- Systec Inoue
- KOYU
- Design Network
- Passage

Factory construction
- UEKI corporation
- Taihei
- Asahikogyosha
- Rikenkeiki
- Epoch transport

System Design
- DISCO
- SS Techno
- Shibuya Kogyo
- Ishii Tool & Eng.

Invented
- Local Clean Technology

Back-end
- Apic
- Yamada
- Kumamoto Bosei
- Ishida Sangyo

Equipment, Parts, materials
- PRE-TECH
- Litho Tech Japan
- Fujikoshi machine
- Koyo Thermo
- Fuji IMVAC
- Horiba STEC
- Sakaguchi E.H VOC
- Yonekura MFG
- Xevis
- Seinan Industries
- SPP technologies
- Tatsuya Machine
- Haruki Seisakusho
- Aichi system
- Beamtron

Parts, Units
- RIX
- TAZMO
- SMC
- Fujikin
- CKD
- VTEX
- FUJI Tech.
- Edwards Japan
- Kanto Chemical
t

Materials
- NAGASE
- Surpass Industry
- Okamoto Glass
- Komatsu Seiki
- Wide Techno
- Taiyo Nissan
- Hakuto
- Hirose Electric
- Oriental motor
- Dainichi Shoji
- Nitto Reinentu
- Shin-Etsu Polymer
- VIYA
- JEM

Solution
- Ochanomizu PAT
- Takewa PAT
- Sano PAT
- Meico Electronic
- Mitsubishi UFJ Lease & Finance
- Yokogawa Solution Service
- NTT DATA
- Mathematical Systems
- JFE Shoji Electronics
- Hugle Electronics
- Flextronics
- Keiko Kogyo
- Tomoe Shokai
- TEI Solutions

Azbil TOOL TRL

Logic Research
- Fab-less
- RF device tech.

University, Public Sector
- Kyushu Univ.
- Yamaguchi Univ.
- Osaka Univ.
- Kyoto Univ.
- Nagoya Univ.
- Yokohama Nat. Univ.
- Kanazawa Univ.
- Tohoku Univ.
- Hokkaido Univ.
- Akiad Ind. Tech. Center

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R&D: 10 times faster
Investment: 1/1,000

Red are big companies.
131 big companies and ~100 SME.
Minimal fab@AIST

Packaging line
Gate Oxidation
Etcher
Etcher
DRIE
Maskless exposure
Sputter
Coater
Developer
B Diffusion furnace
P Diffusion furnace
Al wet etcher
Resist Remover
Oxide Etcher
RCAstation
Wafer Scanner

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Minimal Device Fabrication History

2012
- Cantilever

2013
- PMOS
- Hybrid

2015
- CMOS
- Ring Oscillator
- Full Minimal

2016
- BGA package
- Full Minimal

Hybrid

MEMS core: cantilever

nMOSFET

pMOSFET

VT

CMOSFET

VSS

VOUT

Ring Oscillator

Ring Oscillator
MOSFET by **Full minimal processes**

fabricated at Semicon Japan 2013.

fabricated on Dec. 4, 2013.

Interface states: $D_{it} \times 7.7 \times 10^{10}$ states/cm$^2$

Utilizing rate @ Semicon Japan 2013

- No. of wafers: 7
- 30 processes (excl. alignment mark forming)
- Avg. total process completed time: 10h25m
- Avg. process availability: 60%

Transfer time
Between machine
2%

Process Idle
38%

Process Availability
60%

Typical developing line
- Fabrication time: 1 month
- Process availability: ~1%

- Wafer transfer time to machine process chamber → 30s

20th Century, Industrial Engines:
- Monolithic Fab (Mega Fab)
- Low-variation large-volume production
- Centralized business group, Intensive risk
- Old tradition business, maker-oriented,
- Deep Valley of Death

→ Paradigm Shifts to 21st century

21st Century, Industrial Engines:
- Small Business, Small Factory (Minimal Fab)
- High-variation low-volume Production
- Contribute to local area, distribute the risk, ICT - Networking
- Smart business, customer-oriented,
- Less Valley of Death

Minimal Fab is a good model.