minimal® Fab

– using half-inch wafers to reduce a fab investment to 1/1,000

June 7, 2017 SEMI EXPO RUSSIA, Moscow

Shiro Hara, Ph.D
AIST, JAPAN

1

Issues in enlarging silicon wafer

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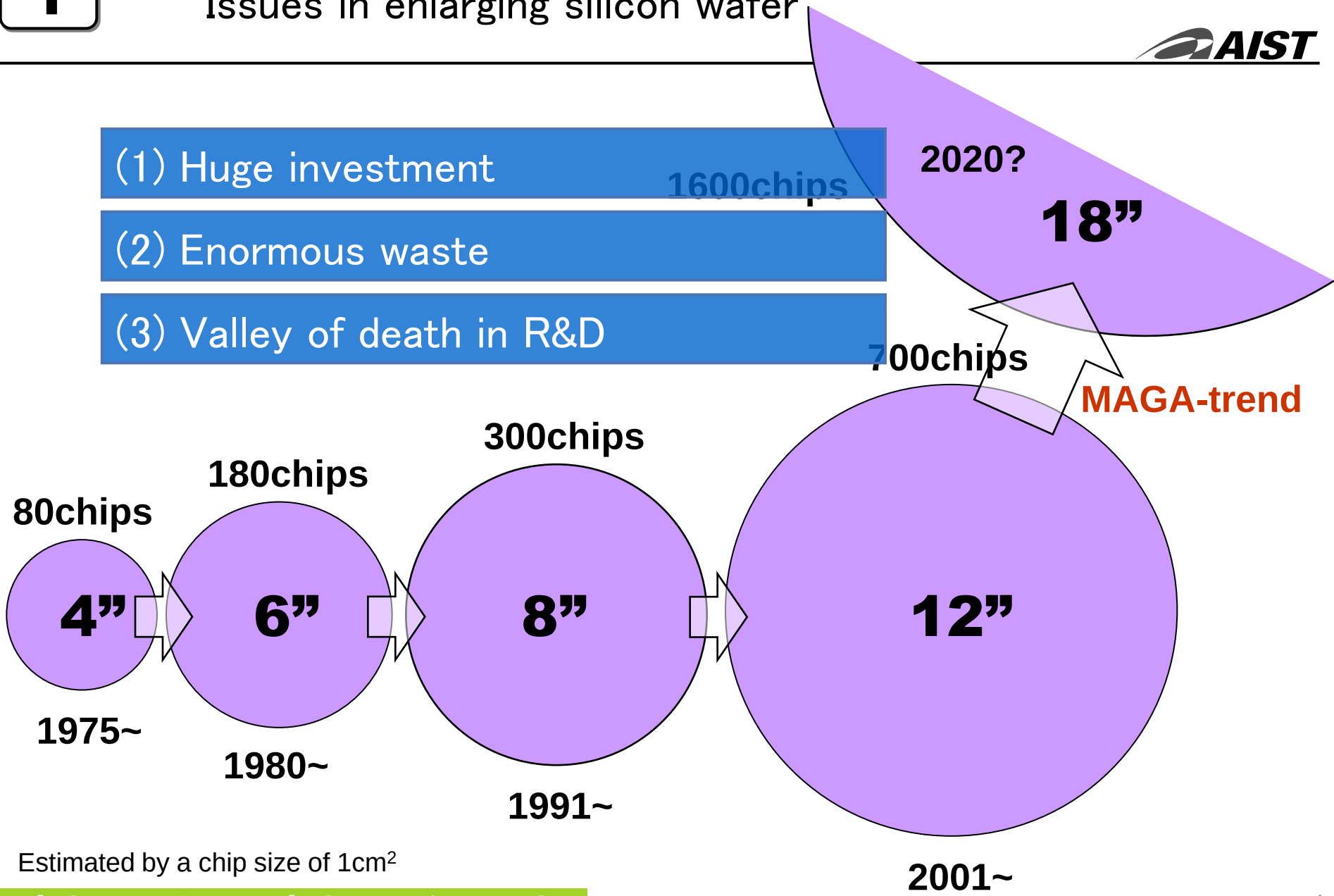
(1) Huge investment

(2) Enormous waste

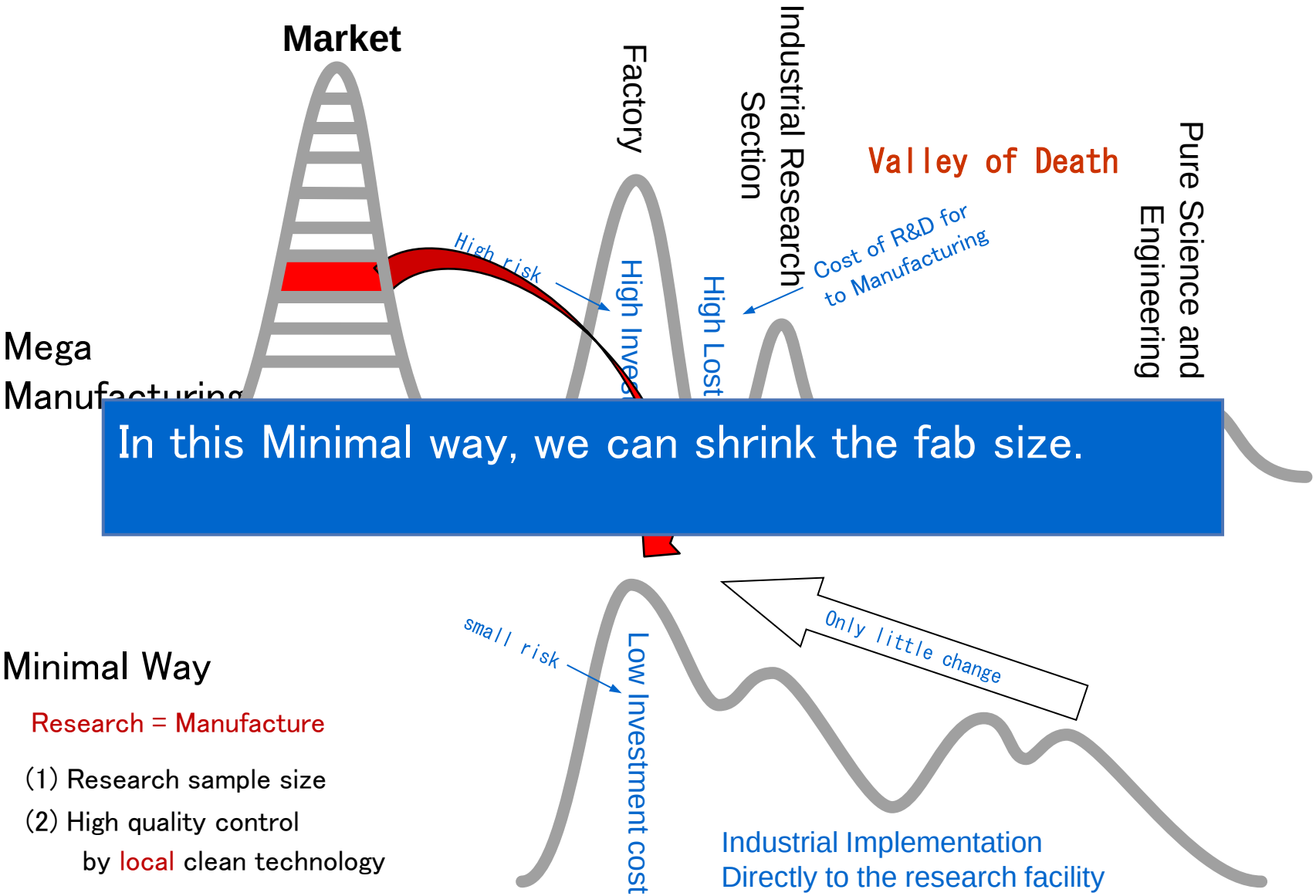
(3) Valley of death in R&D



Estimated by a chip size of 1cm^2

minimal

(3) The Valley of Death in R&D



In this Minimal way, we can shrink the fab size.

Minimal Way

Research = Manufacture

(1) Research sample size

(2) High quality control
by local clean technology

4 To what degree do we shrink the fab size?

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In device fabs,

Number of WIP product types at a certain moment → ～ 1,000 types @ a moment

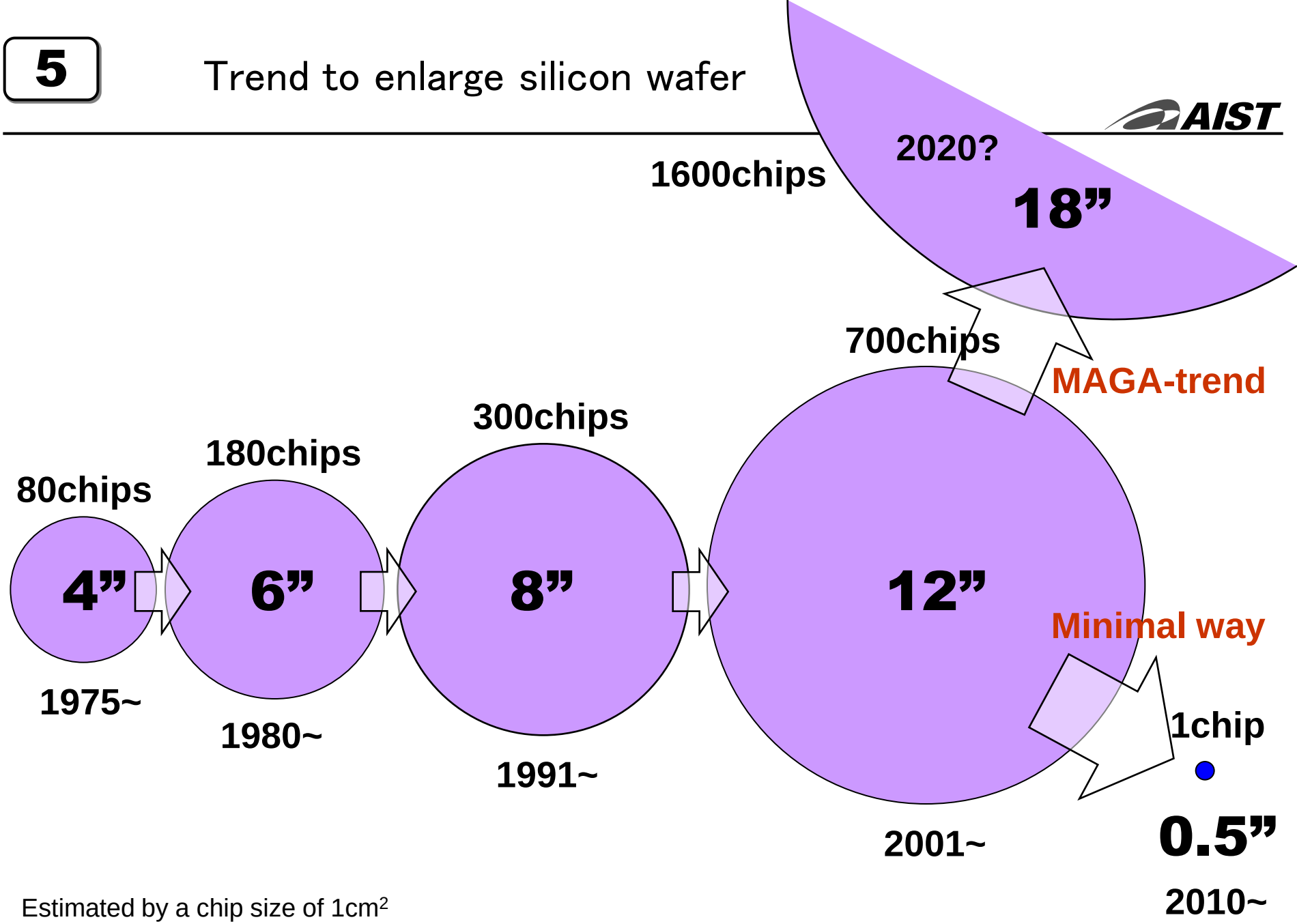
1 type at a certain moment is an ideal fab.

Therefore, we make a fab of 1/1,000.

We call this fab of 1/1,000 "Minimal Fab".

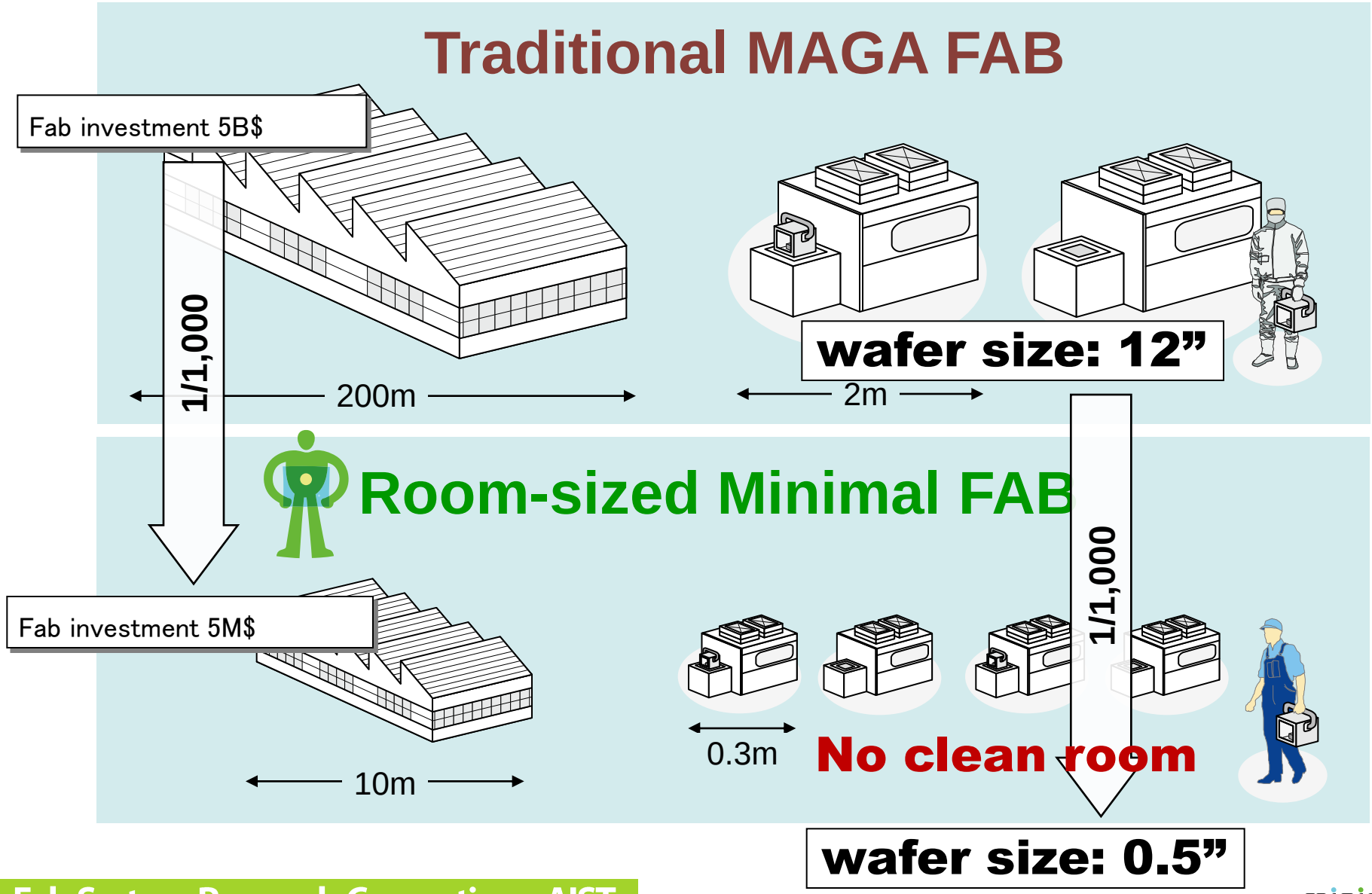
→ We use a tiny wafer intentionally.

Trend to enlarge silicon wafer

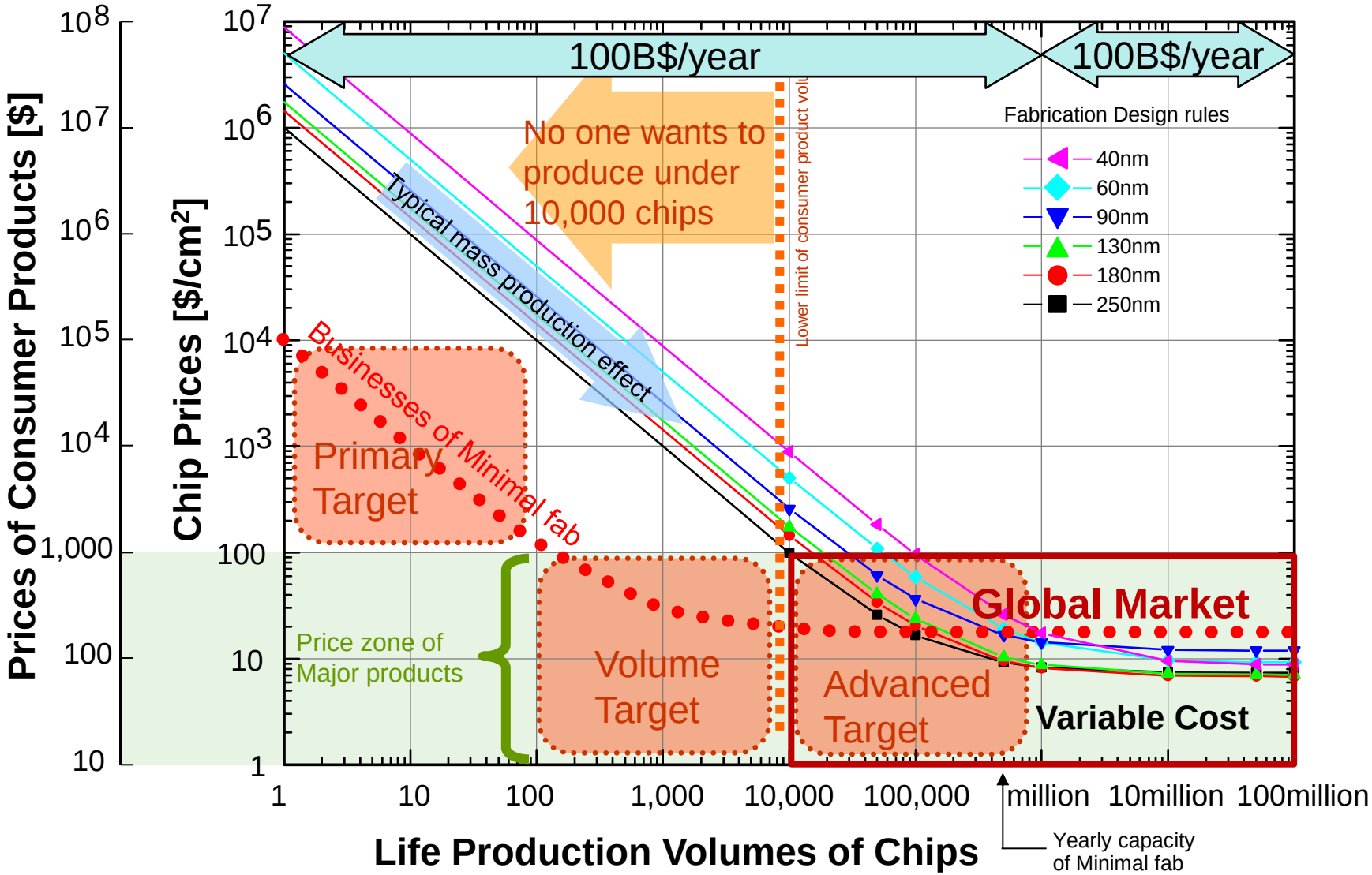


Estimated by a chip size of 1cm^2

Scaling down of fabrication factory



Cost trends for production volumes



8 Standardized Wafer Transfer system

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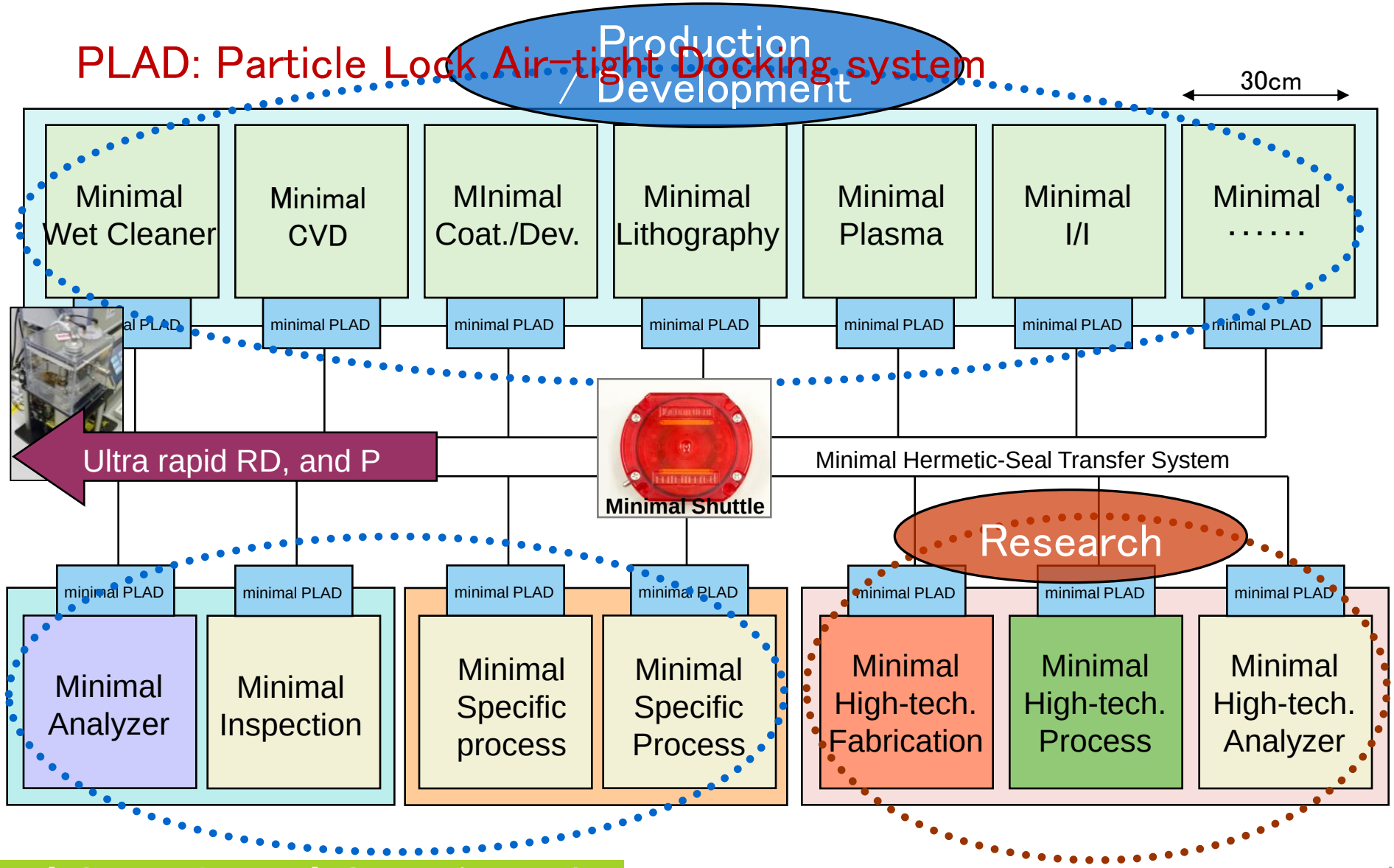
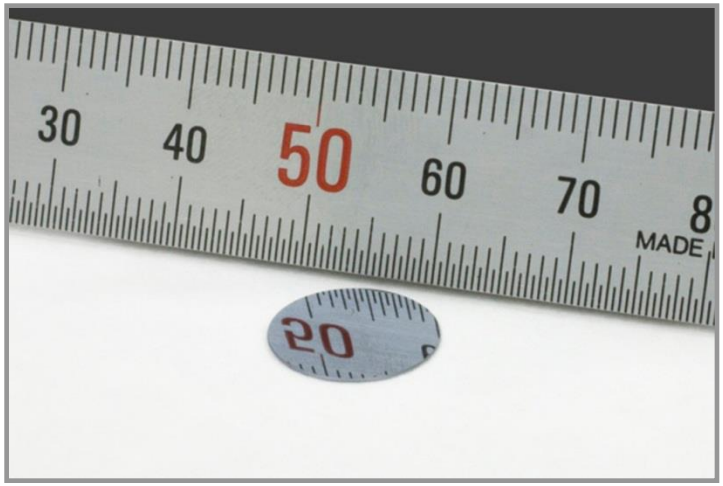
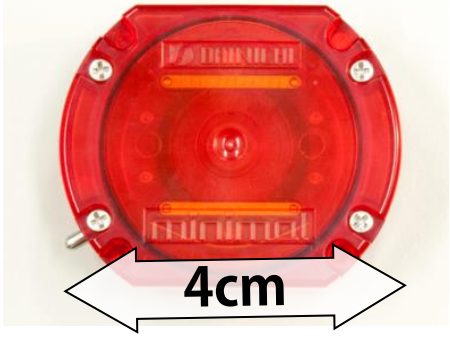


Minimal Tool, Wafer, Shuttle

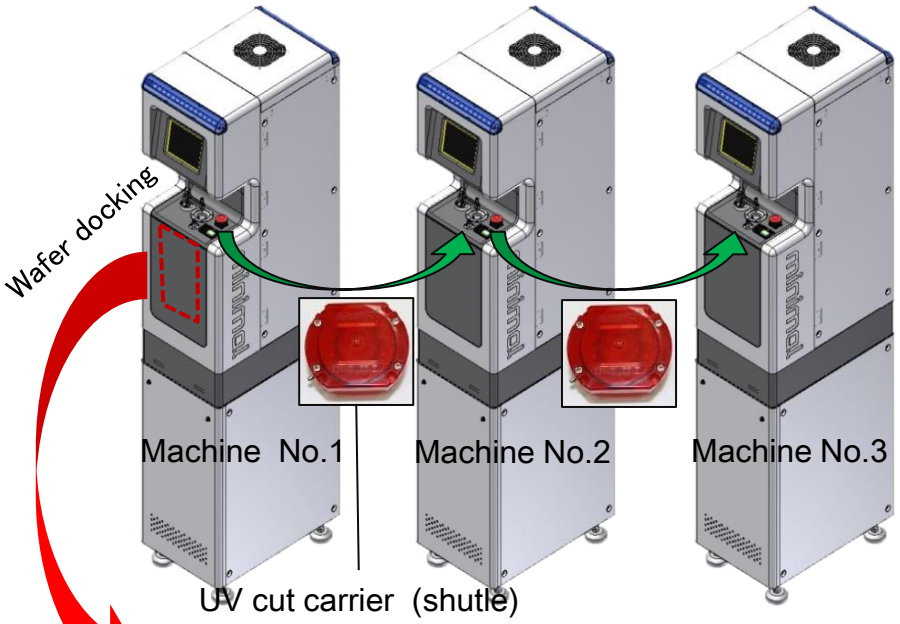
Half inch wafer:
ϕ 12.5mm

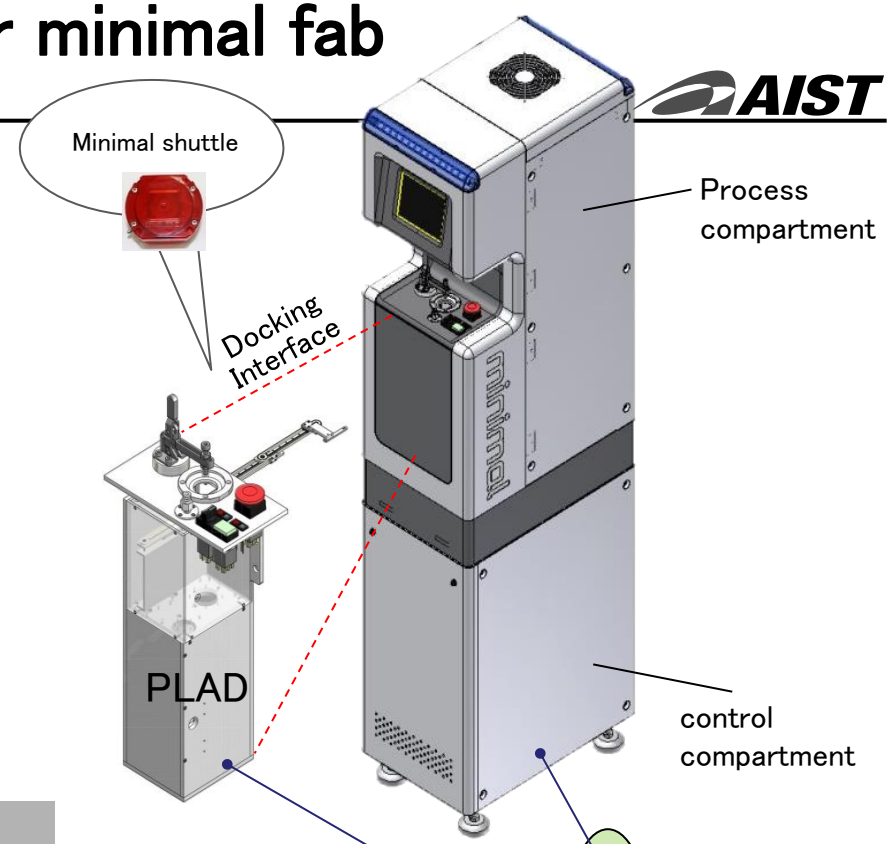


Minimal Shuttle



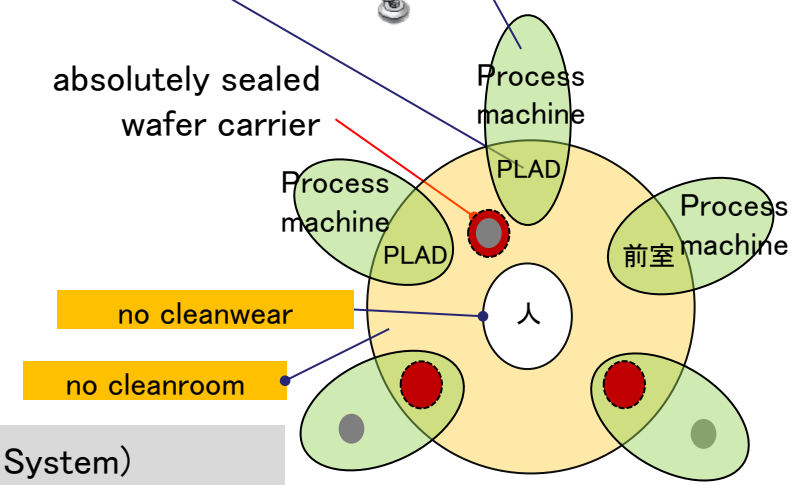
10 Localized clean system for minimal fab





PLAD: Particle Lock Air-tight Docking

A front chamber where particles are absolutely protected during opening process of a shuttle



Localized clean system (EPS: Encapsulated Production System)

Measured Clean level of the system

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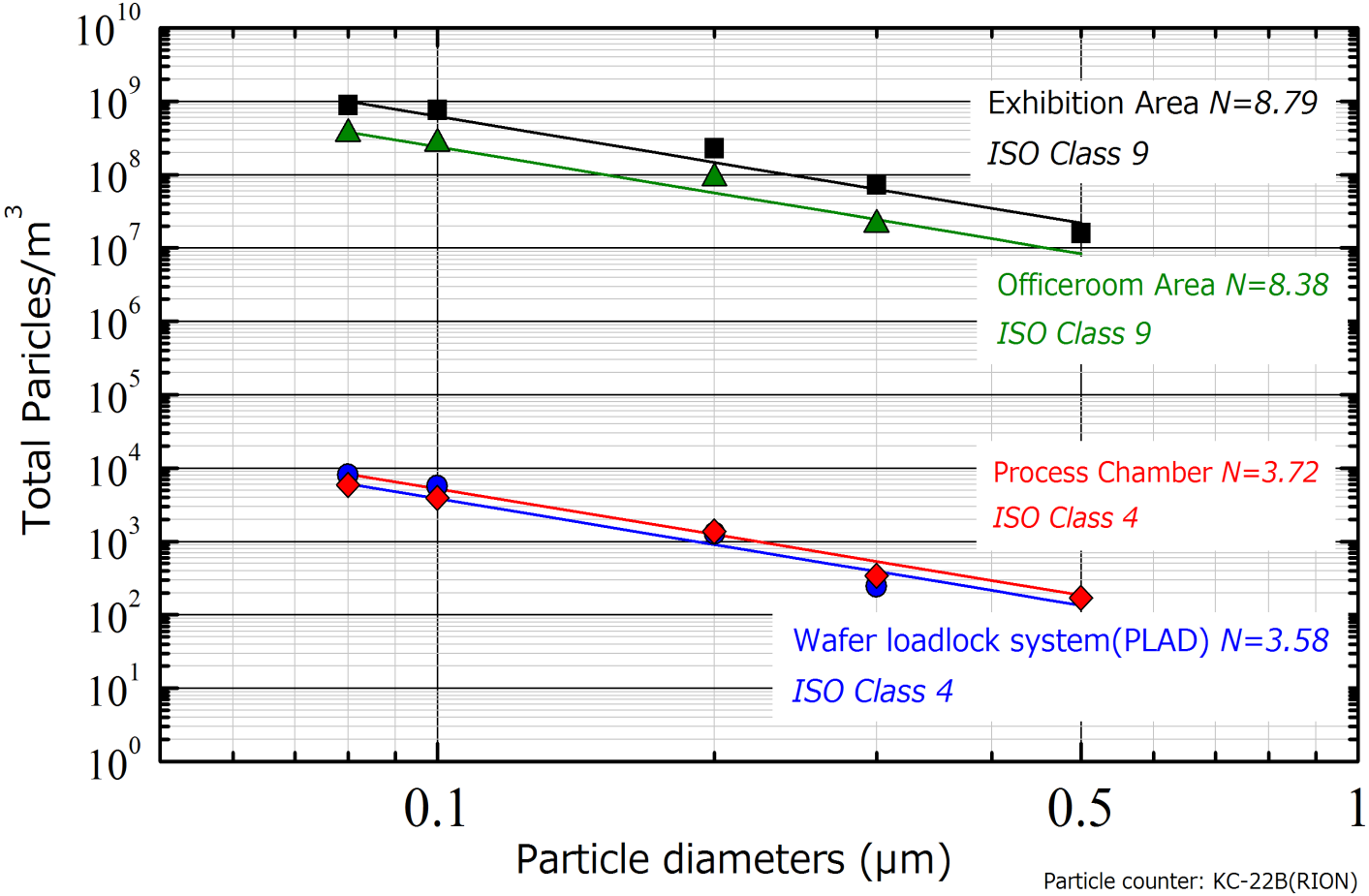
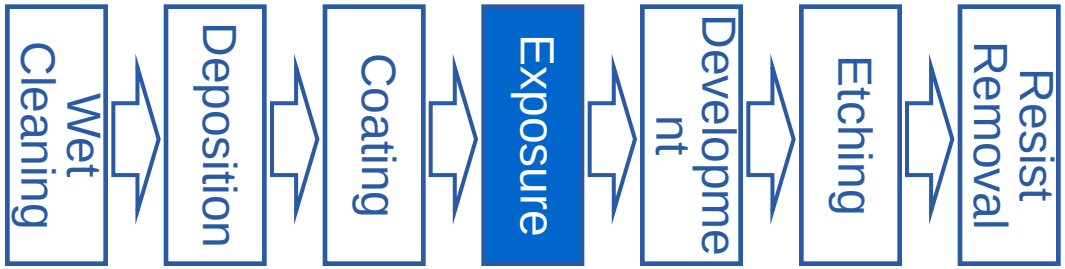
Particle number data of minimal system and environment

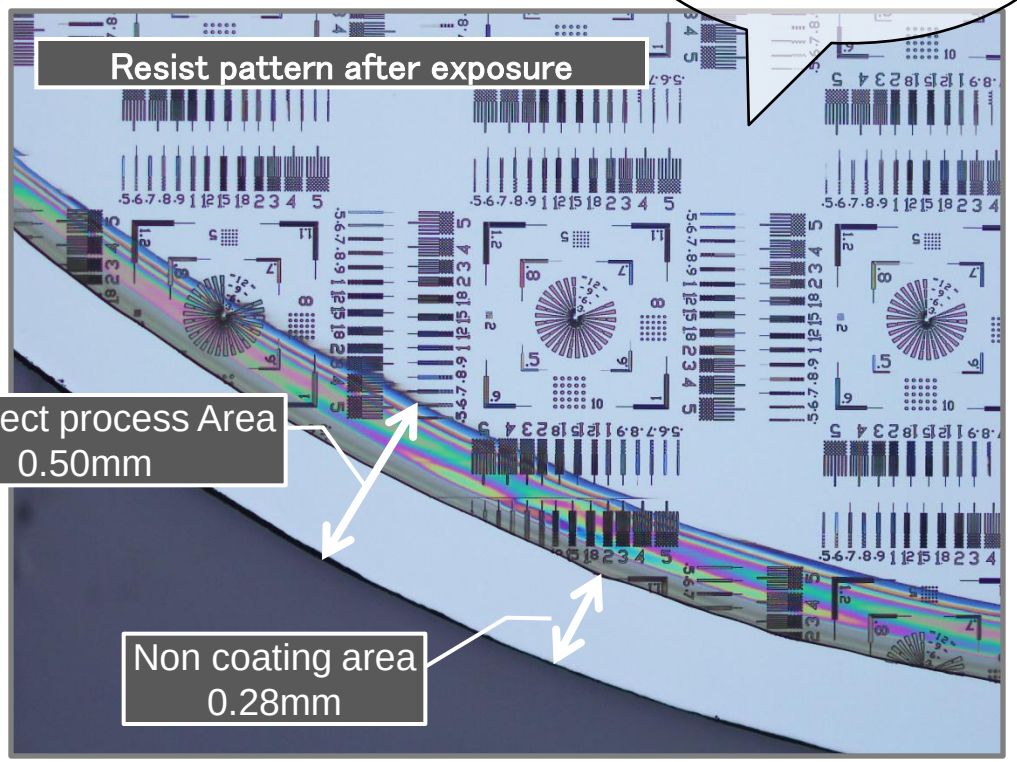


Particle counter: KC-22B(RION)

Mask-less DLP Exposure



No particle without clean room.



Resist: TOK, OFPR-5000 4000rpm, 25sec ~1.00micron, Develop: NMD-3 35sec

R&D&P subjects of minimal fab

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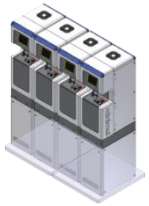
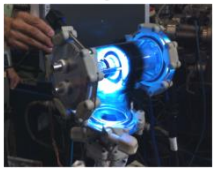
In order to construct a minimal fab,
We have to develop:

[1] Materials, Parts, Modules

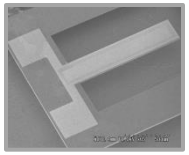
[2] Process equipment



[3] Process technologies



[4] Devices



[5] Factory system

Eco-system in minimal fab

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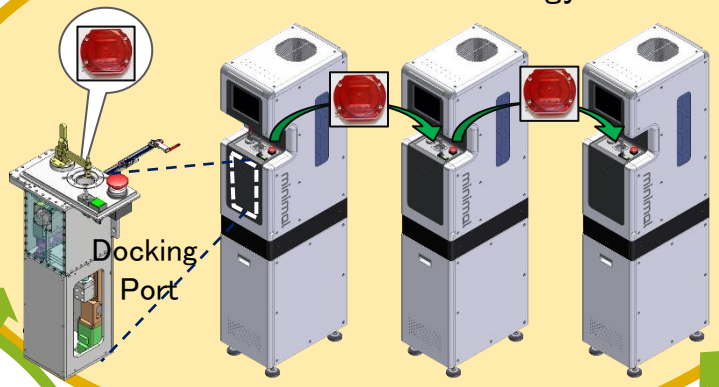
Invented Local Clean Technology



Factory construction
UEKI corporation
Taisei Asahikogyosha
Rikenkeiki
Epoch transport

Minimal Foundry
NEITAS
PMT

Device makers, Minimal Fab Users
Hitachi Toshiba NEC Yokogawa EL Omron
TOKAI RIKA TDK JTEKT Hamamatsu Photonic
Renesas Semi. Manufacturing Murata Manufacturing
Kyowa Electric Instruments
Panasonic Factory Solutions
TAMURA YAZAKI

System Design
Oki Engineering
Digital Electronics
Phenomena Entertainment
Sanyo Systec Inoue KOYU
Yamaha Motor Nanotech
Design Network Passage
Algo system

Back-end
DISCO Apic Yamada
SS Techno Kumamoto Bosei
Shibuya Kogyo
Ishii Tool & Eng.
Adwelds
KAIJO Ishida Sangyo

Equipment, Parts, materials

Equipment
PRE-TECH
Litho Tech Japan
Fujikoshi machinery
Koyo Thermo
ULVAC FUJI IMVAC
YGK Horiba STEC
Sanyou Sakaguchi E.H VOC
Epiquest Yonekura MFG
Xevios Seinan Industries
Sanmei SPP technologies
Riseone Tateyama Machine
KKE Haruki Seisakusho
TCK Japan Science Eng.
PMT STK technology
Aichi system
Beamtron

Parts, Units
RIX
TAZMO
SMC
Fujikin
CKD
VTEX
FUJI Tech.
Edwards Japan
Kashiyama
Hakuto
Hirose Electric
Oriental motor
Dainichi Shoji
Nitto Reinetsu
Shin-Etsu Polymer
VIYIA
JEM

Materials
NAGASE
Surpass Industry
Okamoto Glass
Komatsuseiki
Wide Techno
Taiyo Nissan
Kanto Chemical
Cotec
Shinkouseiki

Logic Research
Fab-less
RF device tech.

Solution
Ochanomizu PAT
Takewa PAT
Sano PAT
Meico Electronic
Azbil
TOOL
TRL
Mitsubishi UFJ Lease & Finance
Yokogawa Solution Service
NTT DATA Mathematical Systems
JFE Shoji Electronics
Hugle Electronics
Flextronics
Keiso Kogyo
Tomoe Shokai
TEI Solutions
DAIWA
Rigaku

University, Public Sector
Kyushu Univ.
Yamaguchi Univ.
Osaka Univ.
Kyoto Univ.
Nagoya Univ.
Yokohama Nat. Univ.
Kanazawa Univ.
Tohoku Univ.
Hokkaido Univ.
Nara Inst. Sci. Tech.
Toyohashi Univ. Tech.
Waseda Univ.
NIMS
NEDIA
Nagano PGIRC.
Akita Ind. Tech. Center
Kanagawa Ind. Tech. Center
Micromachine Center

minimal Fab®
Innovation Platform

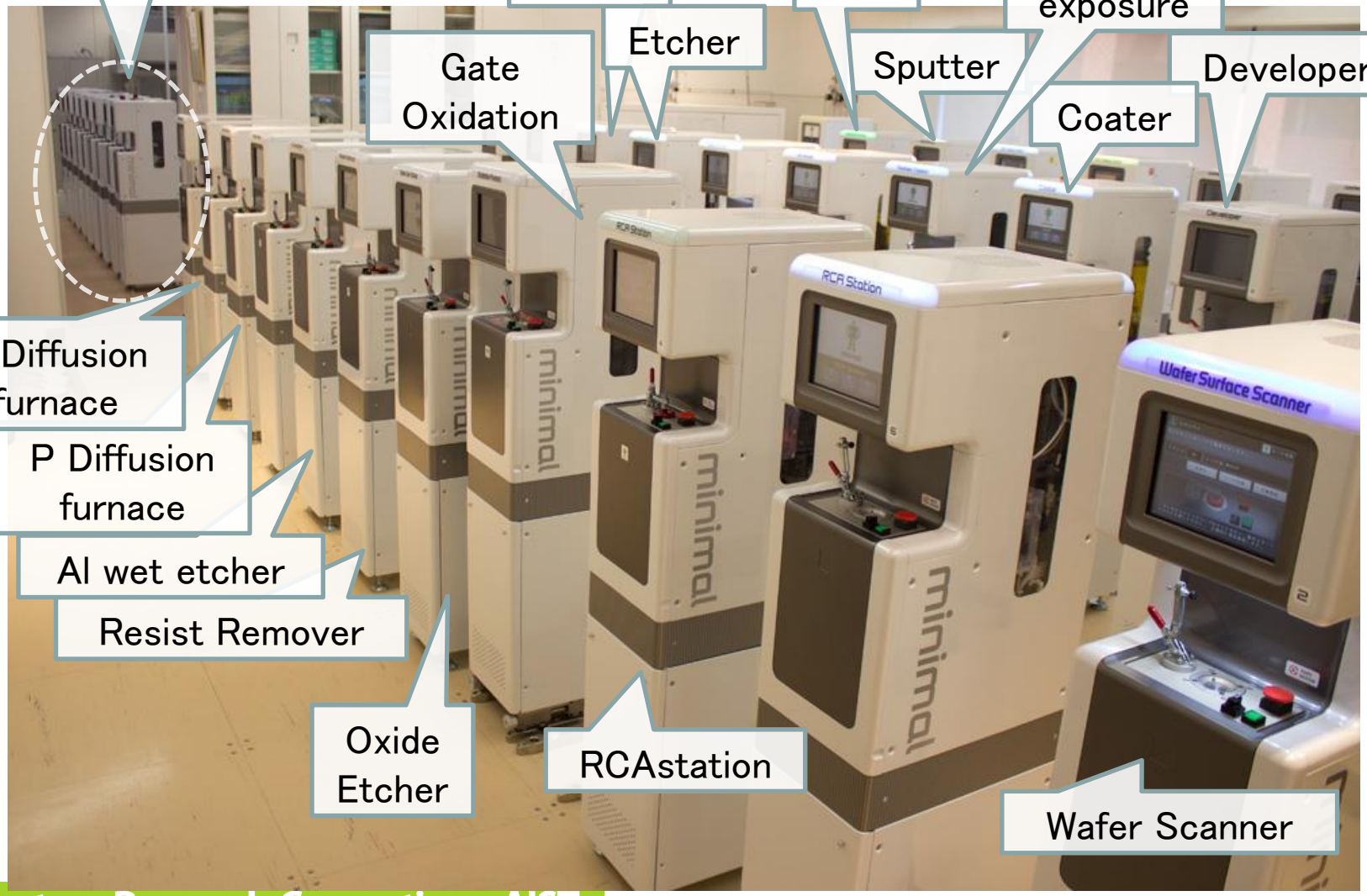
- R&D: 10 times faster
- Investment: 1/1,000

¶ Red are big companies.
¶ 31 big companies and ~100 SME.

Fab System Research Consortium, AIST

August 21, 2016.

Minimal fab@AIST



Minimal Device Fabrication History

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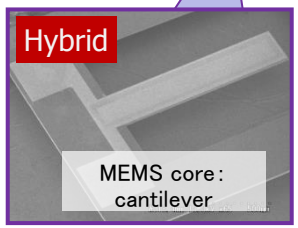
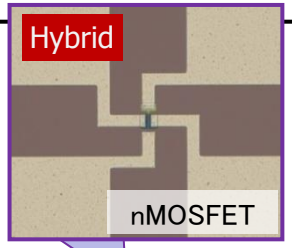
2012

Cantilever



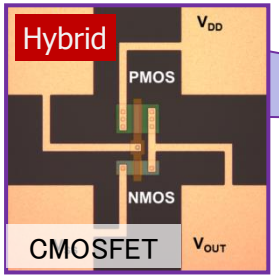
2013

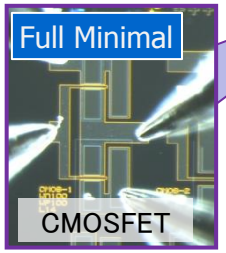
PMOS



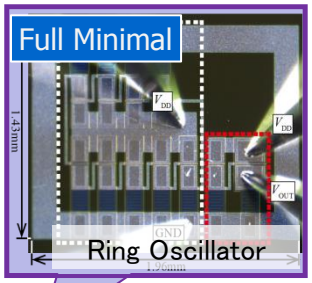
2015

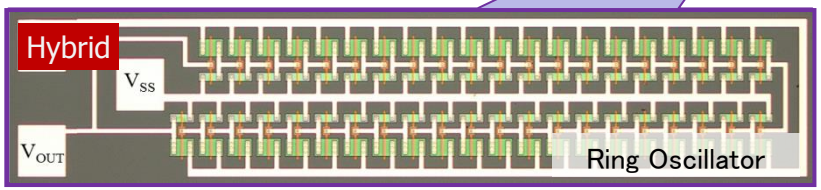
CMOS





Ring Oscillator





2016

BGA package

17 MOSFET by Full minimal processes

fabricated at Semicon Japan 2013.

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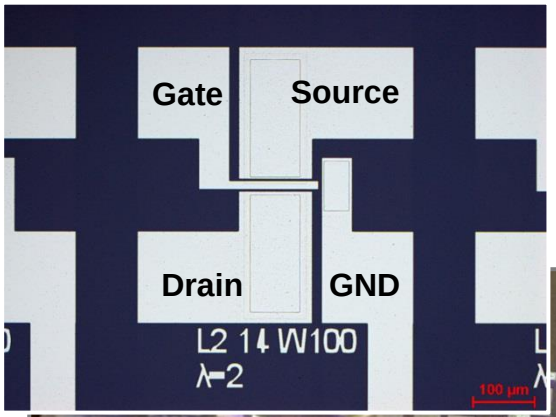
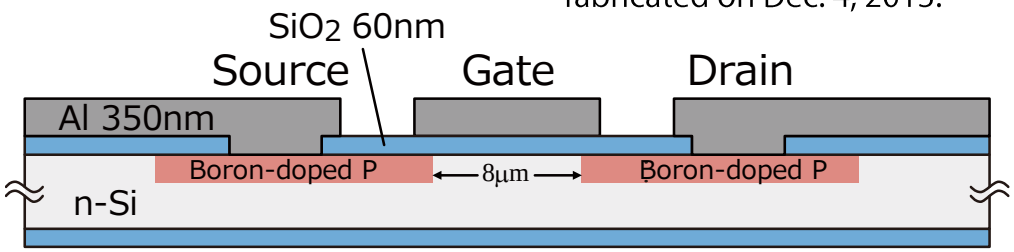
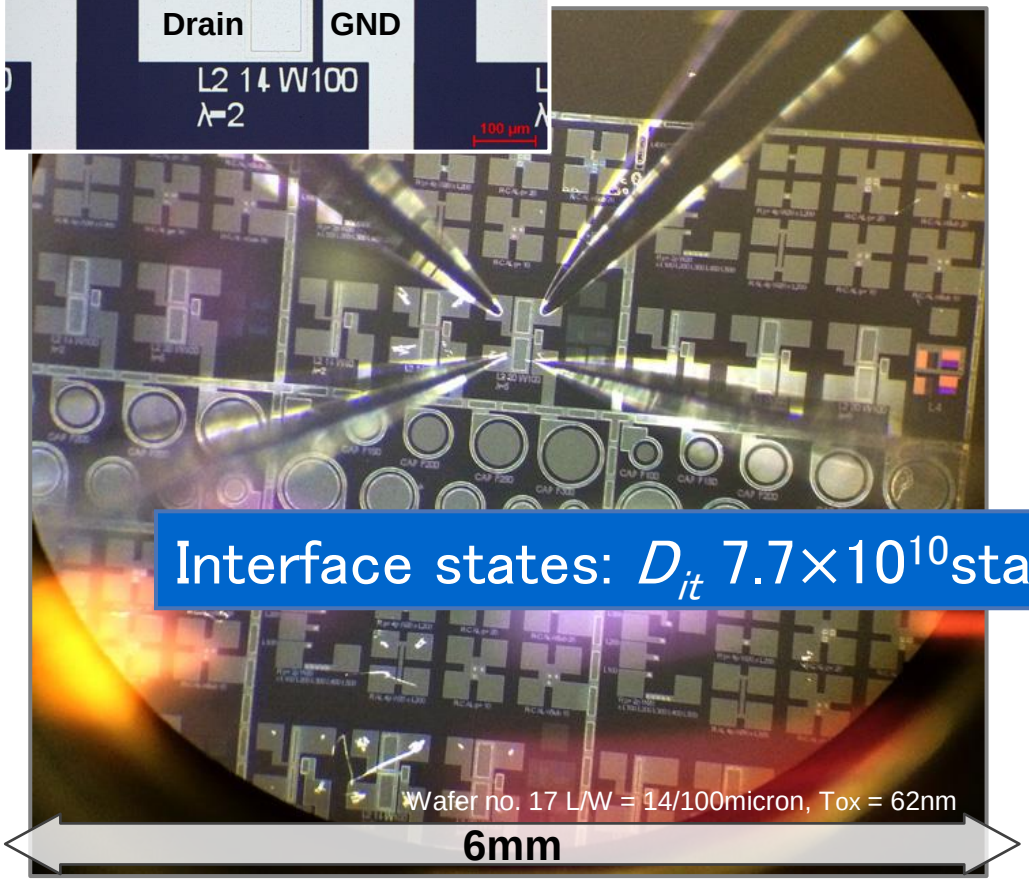


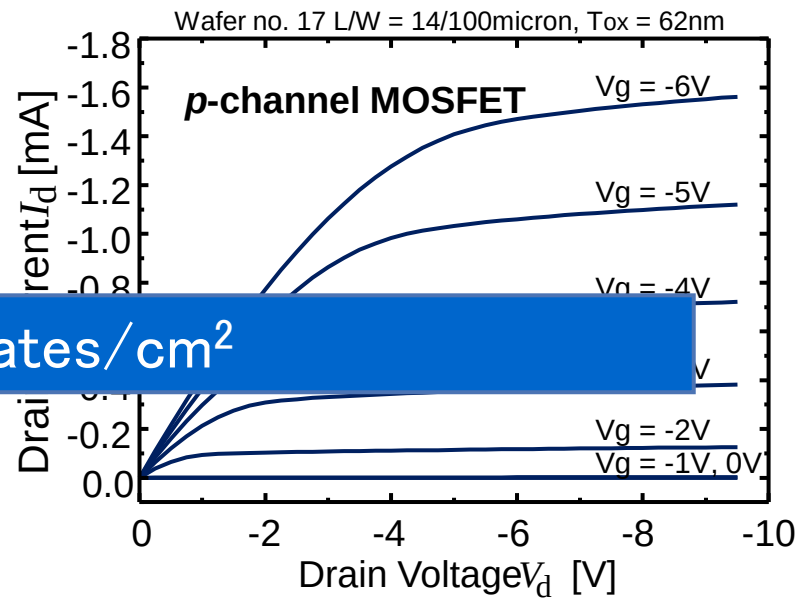
fabricated on Dec. 4, 2013.



7wafers, 35Tr.
→ Yeild100%



Interface states: D_{it} 7.7×10^{10}states/cm^2



S. Khumpuang F. Imura, and S. Hara, "Analyses on Cleanroom-Free Performance and Transistor Manufacturing Cycle Time of Minimal Fab," IEEE Transactions on Semiconductor Manufacturing, 28(4), 551-556 (2015).

Utilizing rate@Semicon Japan 2013

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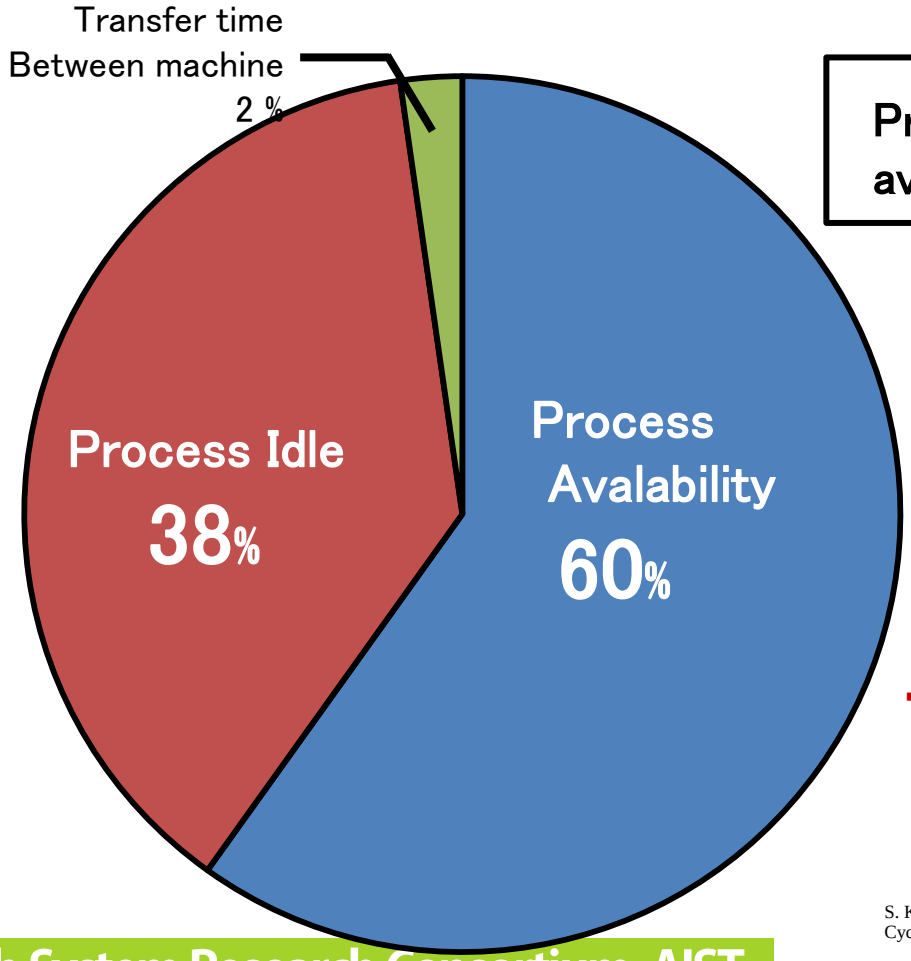
- No. of wafers : 7
- 30 processes
  (excl.alignment mark forming)

- Avg. total process completed time : 10h25m
- Avg. process availability : 60%



$$\text{Process availability(\%)} = \frac{\text{Raw Time}}{\text{complete time}}$$

Typical developing line
- Fabrication time 1 month
- process availability ～1%

- wafer transfer time to machine process chamber → 30s

S. Khumpuang F. Imura, and S. Hara, "Analyses on Cleanroom-Free Performance and Transistor Manufacturing Cycle Time of Minimal Fab," IEEE Transactions on Semiconductor Manufacturing, 28(4), 551-556 (2015).

June 3, 2017.

Roadmap for minimal fab

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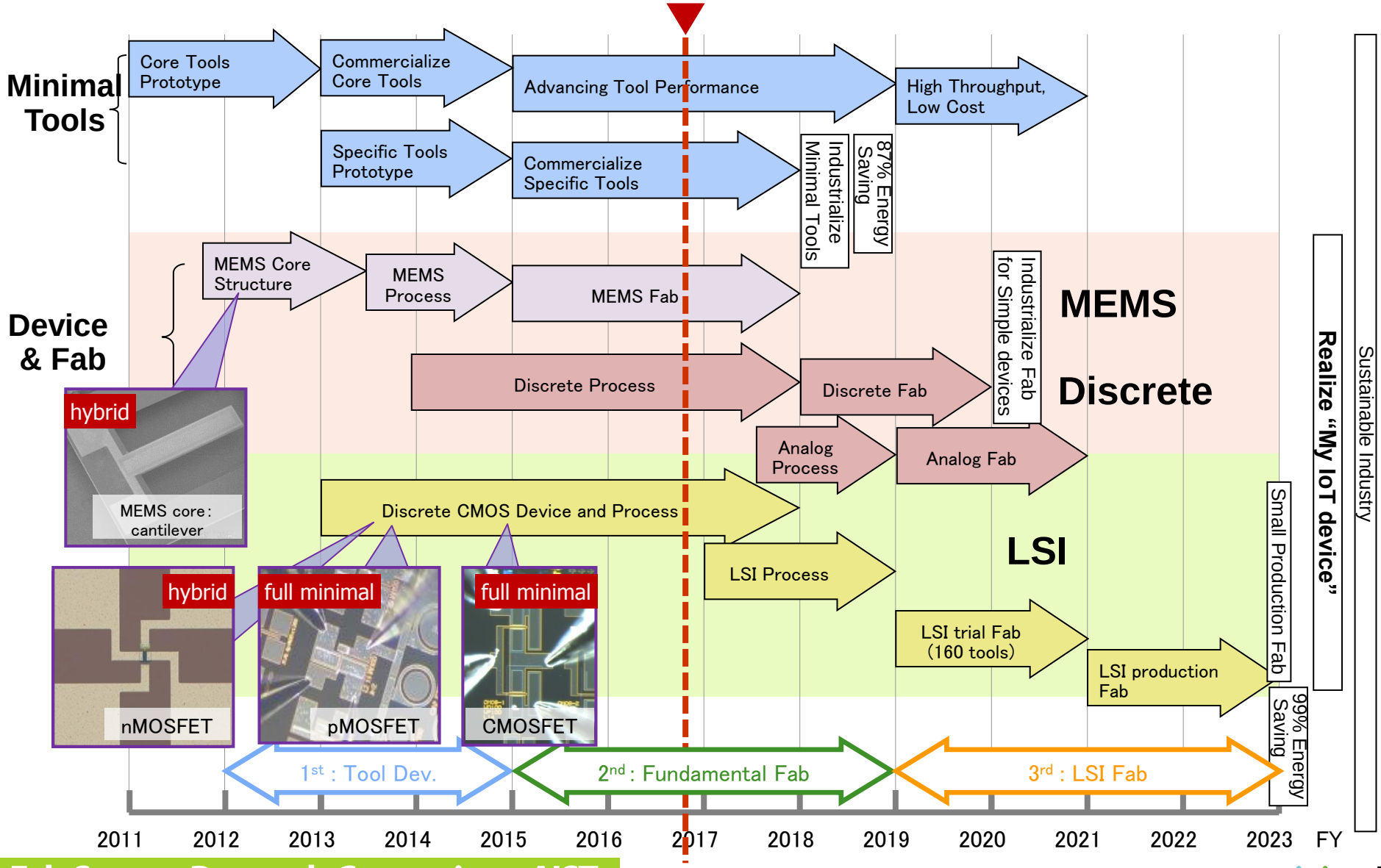

Industrial aspect of minimal fab

AIST

21st Century, Industrial Engines:

- Small Business, Small Factory (Minimal Fab)
- High-variation low-volume Production
- Contribute to local area, distribute the risk, ICT・Networking
- Smart business, customer-oriented,
- Less Valley of Death

Minimal Fab is a good model.

20th Century, Industrial Engines:

- Monolithic Fab (Mega Fab)
- Low-variation large-volume production
- Centralized business group, Intensive risk
- Old tradition business, maker-oriented,
- Deep Valley of Death

→ Paradigm Shifts to 21st century

Industrie 4.0

Advanced Manufacturing (3D printer)